WHAT IS CLAIMED IS

1. An apparatus for branch prediction, comprising:

a history register which stores therein history of previous branch instructions;

an index generation circuit which generates a first index from an instruction address and the history stored in said history register;

a history table which stores therein a portion of the instruction address as a tag and a first value indicative of likelihood of branching in association with the first index;

a branch destination buffer which stores therein a branch destination address or predicted branch destination address of an instruction indicated by the instruction address and a second value indicative of likelihood of branching in association with a second index that is at least a portion of the instruction address; and

a selection unit which makes a branch prediction by selecting one of the first value and the second value.

2. The apparatus as claimed in claim 1, wherein said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if

said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

3. The apparatus as claimed in claim 2, wherein said selection unit predicts no branching if said branch destination buffer does not have an entry therein corresponding to the current instruction address.

4. The apparatus as claimed in claim 1, wherein said index generation circuit generates the first index that is an Exclusive-OR between the history stored in said history register and the current instruction address.

5. The apparatus as claimed in claim 1, wherein more than one said history table is provided so as to allow a plurality of entries to be registered with respect to said first index.

6. A processor, comprising:
a history register which stores therein

history of previous branch instructions;

an index generation circuit which generates a first index from an instruction address and the history stored in said history register;

a history table which stores therein a portion of the instruction address as a tag and a first value indicative of likelihood of branching in association with the first index;

a branch destination buffer which stores therein a branch destination address of an instruction indicated by the instruction address and a second value indicative of likelihood of branching in association with a second index that is at least a portion of the instruction address;

a selection unit which makes a branch prediction by selecting one of the first value and the second value;

an execution control unit which controls execution of instructions; and

an execution operation unit which executes the instructions.

7. A method of branch prediction, comprising the steps of:

providing a history table which stores therein a portion of an instruction address as a tag and a first value indicative of likelihood of branching in association with a first index that is generated from the instruction address and history of pervious branch instructions;

providing a branch destination buffer which stores therein a branch destination address of an instruction indicated by the instruction address and a second value indicative of likelihood of

branching in association with a second index that is at least a portion of the instruction address

selecting one of a first value and a second value; and

predicting branching in response to the selected one of the first value and the second value.

8. The method as claimed in claim 7, wherein said step of selecting one of the first value and the second value selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

9. The method as claimed in claim 8, further comprising the steps of:

registering the current instruction address in said branch destination buffer if said branch destination buffer does not have an entry therein corresponding to the current instruction address; and

registering information about the current instruction address in the history table if said branch destination buffer has an entry therein

corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history and if a prediction made based on the second value turns out to be erroneous.

10. The method as claimed in claim 9, wherein the information about the current instruction address is not registered in said history table if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history and if the prediction made based on the second value turns out to be correct.

11. An apparatus for branch prediction, comprising:

a history register which stores therein history of immediately preceding branch instructions;

an index generation circuit which generates a first index that is an Exclusive-OR between an instruction address and the history stored in said history register;

a history table which stores therein a portion of the instruction address as a tag and a first value indicative of likelihood of branching in association with each said first index;

a branch destination buffer which stores

therein a portion of the instruction address as a tag, a branch destination address of an instruction indicated by the instruction address, and a second value indicative of likelihood of branching in association with each second index that is a portion of the instruction address; and

a selection unit which makes a branch prediction by selecting one of the first value and the second value, wherein said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.